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**DRIVE FOR ACTIVE MATRIX CHOLESTERIC LIQUID CRYSTAL  
DISPLAY**

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## **DRIVE FOR ACTIVE MATRIX CHOLESTERIC LIQUID CRYSTAL DISPLAY**

### **FIELD OF THE INVENTION**

5                   The present invention relates to a drive for an active matrix  
cholesteric liquid crystal display.

### **BACKGROUND OF THE INVENTION**

                  It is well known that cholesteric (also referred as chiral nematic)  
10   liquid crystal displays have optically distinct states: a planar state that reflects  
light, a focal conic state, and a homeotropic state that appears black if a black  
layer is painted on one side of the display. In the following, the planar state is also  
referred as the on-state, and the focal conic state as the off-state. Both the planar  
and the focal conic states are stable at zero voltage. The homeotropic state can  
15   only be maintained with a voltage applied across the display. Thus using the  
planar and focal conic states, cholesteric liquid crystal displays can be  
advantageously addressed by a passive matrix for many applications.

                  However, passive matrix addressed cholesteric liquid crystal  
displays have problems such as cross-talk, long frame times, and black bar  
20   artifacts. These problems can be overcome by driving the displays with an active  
matrix drive scheme at the higher expense of the active matrix. With the intense  
research and development of amorphous and poly silicon thin film transistors,  
active matrix drive appears to be affordable for use in high performance  
cholesteric liquid crystal displays. Organic thin film transistors fabricated on  
25   plastic substrates offer higher voltage outputs (e.g. 100 volts or more) that can be  
used to drive liquid crystal displays that require a high drive voltage.

                  A typical active matrix pixel drive is shown in Fig. 1 and includes a  
matrix of data **10** and select **12** lines. Data and select lines are also called column  
and row lines, respectively. An array of pixels **14** are connected to the data and  
30   select lines through active switching elements that in one example include a

transistor **16** and a storage capacitor **18**. The active matrix addressed liquid crystal display further includes a common electrode **20** connected to all of the pixels.

Nahm et al., **Amorphous Silicon Thin-Film Transistor Active-Matrix Reflective Cholesteric Liquid Crystal Display**, *Proceedings of the 18th International Display Research Conference*, pp. 979-982, 1998, and Kawata et al., **A High Reflective LCD with Double Cholesteric Liquid Crystal Layers**, *Proceedings of the 17th International Display Research Conference*, pp. 246-249, 1997, proposed active matrix addressed bistable cholesteric liquid crystal displays that were operated between the planar and homeotropic states.

10 US 2001/050666 A1 issued December 13, 2001 to Huang et al. discloses active matrix addressed bistable cholesteric liquid crystal displays that made better use of the bistability of the cholesteric liquid crystal display and were operated between the planar and focal conic states. They propose driving the active matrix addressed bistable cholesteric liquid crystal displays by a multiple  
15 level voltage driver that supplies two voltage levels (+40 volts, -40 volts) to achieve the planar state, and another two voltage levels (+30 volts, -30 volts) to obtain the focal conic state.

As shown in Fig. 2, Huang et al. employ row, column, backplane, and pixel voltage waveforms varying with time  $t$  in two consecutive frames.  
20 Without loss of generality, two row voltage waveforms (also referred as select voltage waveforms)  $V_{row1}$ ,  $V_{row2}$  and two column voltage waveforms (also called data voltage waveforms)  $V_{col1}$ ,  $V_{col2}$  are used to illustrate the idea. In the first frame **30**, a select voltage pulse **200** is sequentially applied to row 1 and row 2. In the meantime, data voltage waveforms  $V_{col1}$ ,  $V_{col2}$  are applied to column 1 and  
25 column 2. Note that the data voltage waveforms take different amplitudes in order to achieve distinct optical states. In particular, a voltage pulse of 40 volts is applied to obtain a planar state, and a pulse of 30 volts to obtain a focal conic state. The backplane is connected to zero voltage. The row voltage for selection is preferably about 5 V and, most preferably, at least 5 V higher than column  
30 voltage, in order to open or close the transistor **16**. The pixel voltage  $V_{p11}$  formed

at the intersection of row 1 and column 1 thus is 40 volts, and the pixel voltage  $V_{P22}$  formed at the intersection of row 2 and column 2 is 30 volts.

In the second frame 32, the backplane is set at 40 volts. The data voltage is zero for the planar state, and 10 volts for the focal conic state. The pixel voltage is then either -40 volts for  $V_{P11}$ , 0 volts for  $V_{P12}$ , or -30 volts for  $V_{P22}$ . The zero pixel voltage  $V_{P12}$  keeps the state of the pixel unchanged.

Overall, in the prior art active matrix addressed cholesteric liquid crystal displays, more than 2 different voltage levels in addition to a zero level are required to apply to data voltage waveforms and pixel voltage waveforms. This complexity hinders the use of the active matrix to address cholesteric liquid crystal displays.

It is well known that fewer voltage level drivers would result in a lower cost. A two level voltage driver has been utilized for a passive matrix cholesteric liquid crystal display, such as disclosed by Rybalochka et al., **Dynamic Drive Scheme for Fast Addressing of Cholesteric Displays**, SID 2000, pp. 818-821 and **Simple Drive Scheme for Bistable Cholesteric LCDs**, SID 2001, pp. 882-885. They proposed  $U/\sqrt{2}$  and  $U/\sqrt{3/2}$  dynamic driving schemes requiring only 2-level column and row drivers, which output either  $U$  or 0 voltage, to generate a 3-level pixel voltage including  $+U$ ,  $-U$ , and 0. The passive matrix 3-level drive schemes employ multiple phases, including preparation, holding, selection, and evolution phases. Since active matrix displays do not employ multiple phases as discussed in the above cited papers, it is not apparent whether or how a 3-level drive scheme could be used with an active matrix to obtain the inherent advantages of a 3-level drive scheme.

Therefore, there is a need for an improved drive scheme for an active matrix addressed cholesteric liquid crystal display having fewer voltage levels to reduce complexity of the drive scheme while achieving high optical performance.

## SUMMARY OF INVENTION

The need is met according to the present invention by providing a method of driving an active matrix cholesteric liquid crystal display that includes a matrix of data and select lines and an array of pixels connected to the data and select lines through active switching elements, a pixel being capable of producing two or more gray levels. The method includes providing a select voltage and a plurality of data voltages, and during a pixel writing cycle, applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels 0, +U and -U, having respective duty cycles and controlling the duty cycles of the pixel voltage levels to determine the gray levels of the pixels, and wherein the average voltage applied to a pixel during the pixel writing cycle is zero.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic circuit diagram of a typical prior art active matrix drive;

Fig. 2 is a voltage waveform diagram for driving an active matrix cholesteric liquid crystal display according to the prior art;

Fig. 3A is a voltage waveform diagram for driving an active matrix cholesteric liquid crystal display according to the present invention;

Fig. 3B is a voltage waveform diagram for driving an active matrix cholesteric liquid crystal display according to an alternative embodiment of the present invention;

Fig. 4A is a voltage waveform diagram for driving an active matrix cholesteric liquid crystal display according to an alternative embodiment of the present invention;

Fig. 4B is a voltage waveform diagram for driving an active matrix cholesteric liquid crystal display according to an alternative embodiment of the present invention;

Fig. 5 is a pixel voltage waveform resulting from the drive scheme of Figs. 4A and 4B; and

Fig. 6 is experimental data showing the reflectance response of a cholesteric liquid crystal display to the pixel voltage shown in Fig. 5.

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### DETAILED DESCRIPTION OF THE INVENTION

The present description is directed in particular to elements forming part of, or cooperating more directly with, apparatus and methods in accordance with the invention. It is to be understood that elements not specifically shown or described may take various forms well known to those skilled in the art.

Referring to Fig. 5, a single repetitive unit having only three levels 0, +U, and -U in two frames 30 and 32 is used to generate pixel voltage waveforms according to the present invention. The waveforms can be used to drive cholesteric liquid crystals into various states by providing respective duty cycles and controlling the duty cycles of the pixel voltage levels to determine the final states that result in the gray levels of the display. The on-state and off-state pixel voltage waveforms switch the pixel into final planar and focal conic states, respectively. In one example, the on-state pixel voltage waveform  $V_{Pon}$  has 100% duty cycle, being +U in the first frame 30, and -U in the second frame 32. To minimize the amplitude of U,  $V_{Pon}$  is preferred to have a duty cycle close or equal to 100%. The off-state pixel voltage waveform has a duty cycle determined by  $2T_1/T$ , where T is the period of the waveform, and  $2T_1$  is the total time for the voltage level to be at  $\pm U$  in a single repetitive unit. As shown, the off-state pixel voltage waveform may take various forms including but not limited to  $V_{Poff1}$ ,  $V_{Poff2}$ , or  $V_{Poff3}$ , each of which has a duty cycle determined by experimental data. A typical usable duty cycle for the off-state is between 20% to 50%. In either case, the average voltage applied to a pixel during a single repetitive unit and thus the full pixel writing cycle (which includes one or more repetitive units) is zero.

By properly choosing voltage level U, period T (or frequency  $1/T$ ), and number of the repetitive units, experimental data generated by the inventor,

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show that it is possible to use the simplified pixel voltage waveforms having only 0, +U, and -U, for active matrix addressed cholesteric liquid crystals.

Referring to Fig. 6, the duty cycle dependence of the reflectance of a cholesteric liquid crystal display at the peak wavelength is plotted. The curves through the diamonds and squares correspond to the initial states being the planar and focal conic states, respectively. The data shows that at a high duty cycle from 90% to 100%, the first optical state with high reflectance can be achieved, and at a lower duty cycle from 20% to 50%, the second optical state with lower reflectance can be achieved. The display sample was made according to the method disclosed in US 6,423,368 issued July 23, 2002 to Stephenson et al., which is incorporated herein by reference. The voltage U used in the experiment was 120 volts, mainly determined by the thickness and composition of the liquid crystal layer. The liquid crystal material was dispersed in a polymer binder such as gelatin that did not respond to an electric field. The thickness of the liquid crystal layer was about 9 microns. It is possible that a cholesteric liquid crystal display with less polymer, or without polymer, would have a reflectance response to the duty cycle at a lower voltage level U similar to that shown in Fig. 6. Though the voltage level U is high (around 120 volts) in the example shown in Fig. 5, a driver can be implemented by organic thin film transistors. In addition, a low voltage liquid crystal display with a maximum voltage around 40 volts as disclosed in US 2001/050666 A1 issued December 13, 2001 to Huang et al., can be addressed by the drive schemes disclosed in the present invention.

Based on the experimental study, the present invention proposes a new active matrix addressed cholesteric liquid crystal display drive scheme that reduces the complexity of the prior art drive schemes. Referring to Fig. 3A, in the first frame 30, a zero voltage is applied to the common electrode so that the backplane voltage  $V_{Bp}$  is zero. Row 1 and Row 2 receive select voltage waveforms  $V_{Row1}$  and  $V_{Row2}$ , respectively. The absolute level of the row voltages are not critical, and merely need to be sufficient to drive the transistor 16. Like the discharge voltage pulse 220 in the prior art scheme shown in Fig. 2, the present

invention provides a discharge voltage pulse 320. The discharge voltage pulse 320 discharges the pixel to zero voltage relative to the backplane voltage.

However, in the present invention there are a plurality of select voltage pulses in addition to the discharge voltage pulse in a single frame. As shown in Fig. 3A, the  
5 select waveforms  $V_{Row1}$  and  $V_{Row2}$  have at least two select voltage pulses 300 and 310. The first select voltage pulse 300 is a selection portion to select a line to be addressed, and the second select voltage pulse 310 is a duty cycle portion wherein the duty cycle of the non zero pixel voltages are determined. Similarly, there are two data voltage pulses 360 and 365 for the first optical (planar) state, and two  
10 data voltage pulses 370 and 375 for the second optical (focal conic) state. In particular, the first data voltage pulses 360 and 370 are identical having the same amplitude of +U for both the first and second states. It is the second data voltage pulse 365 or 375 that dictates the final state. When the second data voltage pulse has the same amplitude of +U, the pixel voltage  $V_{P11}$  has a larger duty cycle.  
15 However, when the second data voltage pulse has an amplitude of 0, the pixel voltage  $V_{P22}$  has a smaller duty cycle. In either case, the pixel voltage is +U or 0 in the first frame.

In the second frame 32, a non-zero voltage +U is applied to the common electrode, thus the backplane voltage  $V_{Bp}$  is +U. The select voltages  
20  $V_{Row1}$  and  $V_{Row2}$  are the same as those having a selection portion and a duty cycle portion in the first frame. The data voltage waveforms still have two data voltage pulses 380 and 385 for the first optical (planar) state, and two data voltage pulses 390 and 395 for the second optical (focal conic) state, with the first data voltage pulses 380 and 390 being the same as 0, and the second data voltage pulses being  
25 either 0 like data voltage pulse 385 for the planar state, or +U like the data voltage pulse 395 for the focal conic state. Unlike in the first frame, the pixel voltage is either -U or 0 in the second frame.

Fig. 3B shows an alternative embodiment to implement an active matrix addressed cholesteric liquid crystal display drive scheme according to the  
30 present invention. This embodiment is identical to the one shown in Fig. 3A in



the first frame 30. In the second frame 32, the backplane voltage  $V_{BP}$  is zero. The data voltage waveforms still have two data voltage pulses 381 and 386 for the first optical (planar) state, and two data voltage pulses 391 and 396 for the second optical (focal conic) state. Unlike their counterparts as shown in Fig. 3A, the first data voltage pulses 381 and 391 have a level of  $-U$ , and the second data voltage pulses have a level of either  $-U$  like data voltage pulse 386 for the planar state, or 0 like the data voltage pulse 396 for the focal conic state. The pixel voltage, however, is identical to that generated in Fig. 3A, being either  $-U$  or 0 in the second frame.

Fig. 4A shows another alternative embodiment to implement an active matrix addressed cholesteric liquid crystal display drive scheme according to the present invention. First, the select row voltage waveforms  $V_{Row1}$  and  $V_{Row2}$  have two selected voltage pulses 400 and 410, but do not have a discharge voltage pulse corresponding to the prior art pulse 220 in Fig. 2 or pulse 320 in Fig. 3A. By eliminating the discharge voltage pulse, all pixels regardless of whether they need to be switched will be switched, which may consume more power. However, with this scheme it is possible to generate an on-state pixel voltage such as  $V_{P11}$  having a 100% duty cycle, which allows the amplitude of  $U$  to be minimized. This may in turn reduce power consumption. The on-state pixel voltage having a 100% duty cycle can be critical to achieve a high reflectance optical state in view of data shown in Fig. 6. Second, the data voltage levels consist of a zero voltage and two non-zero voltages  $+U$  and  $-U$ . Like the embodiment shown in Fig. 3A, both  $V_{Col1}$  and  $V_{Col2}$  have first identical voltage pulses 460 and 470, respectively. Second voltage pulse 465 in  $V_{Col1}$  has an amplitude of  $+U$ , which causes the pixel voltage  $V_{P11}$  to be  $+U$  with a 100% duty cycle, and results in a planar state.  $V_{Col2}$  has the second voltage pulse 475 having an amplitude of 0, causing the pixel voltage  $V_{P22}$  to be 0 with smaller duty cycle and resulting in a focal conic state. Third, the zero voltage is applied to the common electrode, resulting in the backplane voltage  $V_{BP}$  being at 0 volts in both the first frame 30 and the second frame 32.

In the second frame 32, the select voltages  $V_{Row1}$  and  $V_{Row2}$  are the same as those in the first frame. The data voltage waveforms have two data voltage pulses 480 and 485 for the first optical (planar) state, and two data voltage pulses 490 and 495 for the second optical (focal conic) state, with the first data voltage pulses 480 and 490 being the same as  $-U$ , and the second data voltage pulses being either  $-U$  like data voltage pulse 485 for the planar state, or 0 like the data voltage pulse 495 for the focal conic state. Unlike in the first frame, the pixel voltage is either  $-U$  or 0 in the second frame.

Fig. 4B shows another alternative embodiment to implement an active matrix addressed cholesteric liquid crystal display drive scheme according to the present invention. This embodiment is identical to the one shown in Fig. 4A in the first frame 30. In the second frame 32, the backplane voltage  $V_{Bp}$  is changed to  $+U$  from 0. The data voltage waveforms have two data voltage pulses 481 and 486 for the first optical (planar) state, and two data voltage pulses 491 and 496 for the second optical (focal conic) state. Unlike their counterparts as shown in Fig. 4A, the first data voltage pulses 481 and 491 are the same being 0 volts. The second data voltage pulse 486 has an amplitude of 0 to achieve the planar state, and the second data voltage pulse 496 has an amplitude of  $U$  to obtain the focal conic planar state. All of the pixel voltages resulting from the data voltages and the backplane voltage are identical to those generated in Fig. 4A, being either  $-U$  or 0 in the second frame.

Circuits and systems for generating voltage waveforms to drive cholesteric liquid crystal displays are well known. Examples are found in US Published Patent Application No. 2001/0050666 published by Huang et al. on December. 13, 2001, which is incorporated herein by reference. Huang et al. provide an active matrix display drive system having data generation drivers that provide pulse trains with more than three different voltage levels to the active pixels. In contrast, the present invention uses data generation drivers to generate only three different pixel voltage levels  $U$ ,  $-U$  or 0.

By adding more select voltage and data voltage pulses in a single frame, it is possible to generate multiple duty cycles to the pixel voltage waveforms, thus multiple gray level cholesteric liquid crystal displays can be achieved with active matrix displays having only three levels 0, +U and -U in the  
5 pixel voltages.

The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

## PARTS LIST

|     |   |
|-----|---|
| 10  | data line                                     |
| 12  | select line                                   |
| 14  | pixel   |
| 16  | transistor                                    |
| 18  | storage capacitor                             |
| 20  | common electrode                              |
| 30  | first frame                                   |
| 32  | second frame                                  |
| 200 | select voltage pulse                          |
| 220 | discharge voltage pulse                       |
| 300 | first select voltage pulse                    |
| 310 | second select voltage pulse                   |
| 320 | discharge voltage pulse                       |
| 360 | first data voltage pulse in the first frame   |
| 365 | second data voltage pulse in the first frame  |
| 370 | first data voltage pulse in the first frame   |
| 375 | second data voltage pulse in the first frame  |
| 380 | first data voltage pulse in the second frame  |
| 381 | first data voltage pulse in the second frame  |
| 385 | second data voltage pulse in the second frame |
| 386 | second data voltage pulse in the second frame |
| 390 | first data voltage pulse in the second frame  |
| 391 | first data voltage pulse in the second frame  |
| 395 | second data voltage pulse in the second frame |
| 396 | second data voltage pulse in the second frame |
| 400 | first select voltage pulse                    |
| 410 | second select voltage pulse                   |
| 460 | first data voltage pulse in the first frame   |
| 465 | second data voltage pulse in the first frame  |
| 470 | first data voltage pulse in the first frame   |
| 475 | second data voltage pulse in the first frame  |
| 480 | first data voltage pulse in the second frame  |
| 481 | first data voltage pulse in the second frame  |
| 485 | second data voltage pulse in the second frame |
| 486 | second data voltage pulse in the second frame |

490 first data voltage pulse in the second frame  
491 first data voltage pulse in the second frame  
495 second data voltage pulse in the second frame  
496 second data voltage pulse in the second frame